



**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Ireland et al.

**Serial No.:** 10/034,236

**Filed:** December 28, 2001

**For:** METHOD OF MAKING A CONTACT  
STRUCTURE

**Confirmation No.:** 9992

**Examiner:** H. Tsai

**Group Art Unit:** 2812

**Attorney Docket No.:** 2269-7000.2US  
(95-1141.02/US)

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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

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Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document listed on attached Form PTO/SB/08 be considered by the Examiner and made of record. Copies of any cited foreign patents, publications, or pending unpublished U.S. applications are enclosed pursuant to 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

Other Documents

ITOH, et al., "Two Step Deposited Rugged Surface (TDRS) Storage node and Self Aligned Bitline-Contact Penetrating Cellplate (SABPEC) for 64MbDRAM STC CELL," Date Unknown, 2 pgs, Oki Electric Industry Co., Ltd., VLSI R&D Center, Japan.

Applicants offer to supply any explanation or discussion of the document which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed concurrently with an RCE in the above-identified application, and therefore no additional fee is due.

Respectfully submitted,



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Date: April 14, 2006  
DRJ/sfc:es

Enclosures: Form PTO/SB/08  
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PTO/SB/08B(10-03)

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet

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of

1

**Complete if Known**

Application Number

10/034,236

Filing Date

December 28, 2001

First Named Inventor

Ireland et al.

Group Art Unit

2812

Examiner Name

H. Tsai

Attorney Docket Number

2269-7000 2US (95-1141 02/US)

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		ITOH, et al., "Two Step Deposited Rugged Surface (TDRS) Storage node and Self Aligned Bitline-Contact Penetrating Cellplate (SABPEC) for 64MbDRAM STC CELL," Date Unknown, 2 pgs, Oki Electric Industry Co., Ltd., VLSI R&D Center, Japan.	

Examiner  
SignatureDate  
Considered

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